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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/082,663	05/21/1998	RICHARD L. SOLOMON	97125	2987

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EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	18

DATE MAILED: 03/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/082,663	SOLOMON, RICHARD L.	
	Examiner	Art Unit	
	Thai Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicant's amendment filed on 08/12/2002, and entered on 02/12/2004. Claims 1-45 are now pending.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Each of claims 11 and 12 recites the limitation "the response" in line 1 of claims 11 and 12. There is insufficient antecedent basis for this limitation in the claims.

Claims 31 and 32, each recites the limitation "the response" in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow, Wing-Chi, US patent no. 6,078,742.

As per claim 1, Chow discloses a method and system for emulating data transfer between a bus device and a memory of a system with feature limitations very similar to the claimed invention. According to Chow, the method includes steps

detecting a signal on the bus indicating a request to access the device (col. 4, lines 27-46),

monitoring the bus for a response by the device (col. 3, lines 18-45), and

sending a response to the signal within bus cycles for access without a response being made by the device (col. 4, lines 29-46). Chow does not expressly disclose the feature of a selected period of time passes as claimed.

Practitioner in the art at the time of the invention was made would have found Chow disclosure of the bus cycle for the sending of response would imply the limitation of a selected period of time as claimed because bus cycles in computer processing data is to measure clock time interval (a period of time) usually preselected such that the data processing system would take to process data. In other words, bus cycle in the present data processing system has been designed to represent for a preselected time period so that the data processing would process data in a synchronous manner.

As per claim 2, Chow discloses the bus is a small computer system bus interface (Figs. 4, 9).

As per clam 3, Chow discloses sending a first signal that indicates a presence of the device being emulated on the bus (Fig. 10).

As per claim 4, Chow discloses bus busy signals.

As per claim 5, Chow discloses sending a signal in response to the request (col. 6, lines 33-39).

As per claim 6, Chow discloses sending wait state signal would imply not ready signal for device access and retrieval information.

As per claim 7, Chow discloses a preselected data sequence in the second signal (col. 5, lines 19-27).

As per claims 8 and 10, Chow discloses the claimed limitations for other peripheral bus devices to access to the DMA controller.

As per claim 9, Chow discloses the device would not be present in the data processing system (Figs. 4 and 9).

As per claims 11 and 12, Chow discloses a preset response in the memory access from the bus device, and responses made by the device when the device is present on the bus (col. 2, lines 34-67).

As per claim 13, Chow discloses a state machine implemented in the bus device for monitoring, detecting, and sending responses as claimed (Figs. 9 and 10, col. 5, line 10 to col. 6, line 40).

As per claim 14, Chow discloses a method for emulating a device in a computer system during initialization of an operating system with feature limitations very similar to the claimed invention. According to Chow, the emulation method includes steps:

Monitoring and detecting a signal on the bus indicating a request transaction to access the device (col. 4, lines 27-46),

monitoring the bus for a response by the device (col. 3, lines 18-45), and

sending a response to the signal when bus cycles (time) memory access without a response being made by the device. Chow does not expressly disclose the feature of a selected period of time passes as claimed.

Practitioner in the art at the time of the invention was made would have found Chow disclosure of bus cycle for the sending of response would imply the limitation of a selected period of time in sending and retrieving response because bus cycles in the computer system are to represent time in a preselected manner such that the data processing system would be able to process and access data from memory system in synchronization.

As per claim 15, Chow discloses bus and computer system interface bus as claimed (Figs. 1-4).

As per claim 16, Chow discloses sending a response including a signal that indicates a presence of the device being emulated on the bus (col. 5, lines 2-39).

As per claim 17, Chow discloses bus signals which would include bus busy signals.

As per claim 18, Chow discloses a data processing system for emulation of the device presence in the system bus with feature limitations very similar to the claimed invention. According to Chow, the system includes

a bus (Figs. 1-3),

means for detecting a signal on the bus indicating a request to access the device (col. 4, lines 27-46),

means for monitoring the bus for a response by the device (col. 3, lines 18-45), and

sending a response to the signal within bus cycles intended without a response being made by the device. Chow does not expressly disclose the feature of a selected period of time passes as claimed.

Practitioner in the art at the time of the invention was made would have found Chow disclosure of the bus cycle for the sending of response would imply the limitation of a selected period of time in sending and retrieving response because bus cycle in computer processing data is to measure clock time required in a preselected manner such that the data processing computer would access and operate data within period of time. In other words, bus cycle is time period interval in preselected manner for memory access and read/write operation.

As per claim 19, Chow discloses system bus and bus interface to the system as claimed.

As per claim 20, Chow discloses means for sending signal to indicate a presence of the device on the bus (col. 5, lines 2-39).

As per claims 21-26, Chow discloses bus signals as claimed for accessing to the bus device (Fig. 9, col. 5, line 10 to col. 6, line 40).

As per claim 27, Chow discloses a system for processing data with feature limitations very similar to the claimed invention (Summary of the Invention). According to Chow, the system includes

A bus (Figs. 1-3),

A plurality of devices connected to the bus (Figs. 1-3),

An emulation bus device (Fig. 3, col. 3, lines 20-45), wherein the emulation device includes means

For detecting a signal on the bus indicating a request to access the device (col. 4, lines 27-46) during system initialization,

Means monitoring the bus for a response by the device (col. 3, lines 18-45), and

The emulation system sending a response to the signal in bus cycles for an intended time passes without a response being made by the device. Chow does not expressly disclose the feature of a selected period of time passes as claimed.

Practitioner in the art at the time of the invention was made would have found Chow disclosure of the bus cycle for an intended time for the sending of response would imply the limitation of a selected period of time in sending and retrieving response because bus cycle in computer processing data is to measure clock time representing for a preselected period of time which the CPU computer takes to process data.

As per claims 28-29, Chow discloses the claimed limitations in the bus interface and memory access.

As per claim 30, Chow discloses a system for processing data with feature limitations very similar to the claimed invention (Summary of the Invention). According to Chow, the system includes

A bus (Figs. 1-3),

A plurality of devices connected to the bus (Figs. 1-3),

An emulation bus device (Fig. 3, col. 3, lines 20-45), wherein the emulation device includes means

For detecting a signal on the bus indicating a request to access the device (col. 4, lines 27-46) during system initialization,

Means monitoring the bus for a response by the device (col. 3, lines 18-45), and

The emulation system attached to the bus (Figs. 3 and 9) sending a response to the signal for an intended cycle time without a response being made by the device. Chow does not expressly disclose the feature of within period of time as claimed.

Practitioner in the art at the time of the invention was made would have found Chow disclosure of bus cycle for the sending of response would imply the limitation of within period of time in sending and retrieving response because the bus cycle in data processing computer is used to measure a period of time programmed before or a preselected period of time as claimed in which the CPU and devices attached to the bus in the computer take to access to process data in synchronous order.

As per claims 31-34, Chow discloses bus access signals as claimed (Figs. 9 and 10).

As per claim 35, claims 35 is directed to a computer program product for use with a data processing system for emulating a device for controlling and processing method as in claim 1 above. Chow discloses a computer program product for emulating a device with feature limitations very similar to the claimed invention. According to Chow, the program for emulation of the bus device includes

A computer usable medium to store program instructions for emulation (Figs. 3, 8-9),

Instruction means for detecting a signal on the bus indicating a request to access the device (col. 4, lines 27-46) during system initialization,

Means monitoring the bus for a response by the device (col. 3, lines 18-45), and

The emulation system attached to the bus (Figs. 3 and 9) sending a response to the signal for an intended bus cycle without a response being made by the device. Chow does not expressly disclose the feature of a selected period of time as claimed.

Practitioner in the art at the time of the invention was made would have found Chow disclosure of bus cycle for the sending of response would imply the limitation of within period of time in sending and retrieving response because the bus cycle in data processing computer is used to measure a period of time programmed before or a selected period of time as claimed in which the CPU and devices attached to the bus in the computer take to process data in synchronous order.

As per claims 36-40, Chow discloses bus signals as claimed in bus access operations.

As per claims 41, Chow discloses a method in a data processing system for emulating a device for use within the data processing system with feature limitations very similar to the claimed invention (Summary of the Invention). According to Chow, the emulation method includes steps:

detecting an input/output signal on the bus indicating a request to access the device (Figs. 3, 4, 9, col. 4, lines 27-46),

monitoring the bus for a response by the device to be emulated (col. 3, lines 18-45), and

sending a response to the signal when in bus time cycles for an intended time without a response being made by the device for device emulation. Chow does not expressly disclose the feature of a selected period of time passes as claimed.

Practitioner in the art at the time of the invention was made would have found Chow disclosure of the bus cycle for the sending of response would imply the limitation of a selected period of time as claimed because bus cycle in computer processing data is to measure clock time interval (a period of time) usually preselected such that the data processing system would take to process data. In other words, bus cycle in the present data processing system has been designed to represent for a preselected time period so that the data processing would process data in a synchronous manner.

As per claim 42, Chow discloses prestored data in the response according bus protocol (Figs. 4-9, col. 5, lines 19-27).

As per clam 43, Chow discloses starting a timer for emulation of bus device (Fig. 10).

As per claims 44, Chow discloses the claimed limitations for other peripheral devices as claimed.

As per claim 45, Chow discloses bus access including bus release as claimed.

Response to Arguments

Applicant's arguments with respect to claims 1-45 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Thai Phan whose telephone number is 703-305-3812.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

5. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thai Phan
Mar. 14, 2004

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Patent Examiner
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